VLSI TECHNOLOGY LLC v. INTEL CORP., Appeal No. 2021-1826 (Fed. Cir. November 15, 2022). Before Bryson, Chen, and Hughes. Appealed from the PTAB.

Background:

VLSI sued Intel in district court, alleging infringement of its patent. Intel filed multiple IPRs challenging the asserted claims of VLSI's patent. The Board found all challenged claims to be unpatentable. VLSI appealed, arguing that the Board did not construe two claim features properly.

The claimed features at issue are (1) "a *force region* at least under the bond pad characterized by being susceptible to defects due to stress applied to the bond pad," and (2) "wherein the layout comprises a plurality of metal-containing interconnect layers that extend under a first bond pad of the plurality of bond pads, at least a portion of the plurality of metal-containing interconnect layers underlying the first bond pad and not electrically connected to the first bond pad *as a result of being used for electrical interconnection* not directly connected to the bond pad."

Issues/Holdings:

Did the PTAB err in construing the "force region" feature? No, affirmed. Did the PTAB err in construing the "used for electrical interconnection" feature? Yes, reversed and remanded.

Discussion:

The district court construed the "force region" as a "region within the integrated circuit in which forces are exerted on the interconnect structure when a *die attach* is performed." At the PTAB, the parties agreed in part with this construction but disputed the construction of "die attach." Intel argued for a broad construction that includes any method of attaching a chip to another electronic component, such as wire bonding. VLSI argued for a narrow construction whereby "die attach" only refers to a specific method of attaching, namely, "flip-chip bonding." The PTAB adopted Intel's claim construction.

The Federal Circuit affirmed the PTAB's claim construction due to intrinsic evidence within the patent-in-suit. The specification made clear that the invention was not limited to flip-chip bonding, as wire bonding was specifically disclosed as an example of a die attach. Therefore, a relatively broad claim construction was proper due to the presence of multiple examples of bonding used within the claimed "force region."

Regarding the second claimed feature, the PTAB interpreted the phrase "*used for electrical interconnection* not directly connected to the bond pad" as meaning "interconnect layers that are electrically connected to each other but not electrically connected to the bond pad or to any other active circuitry." VLSI argued that the PTAB's interpretation was too broad.

The Federal Circuit agreed with VLSI. Firstly, the language "used for electrical interconnection" means that the interconnect layers carry electricity. Secondly, the claim also refers to "dummy metal lines" that do not carry electricity. Under the PTAB's claim construction the interconnect layer would be no different from the "dummy metal lines," and redundant claim constructions are disfavored.

Annotated Figure 1 of '552 patent

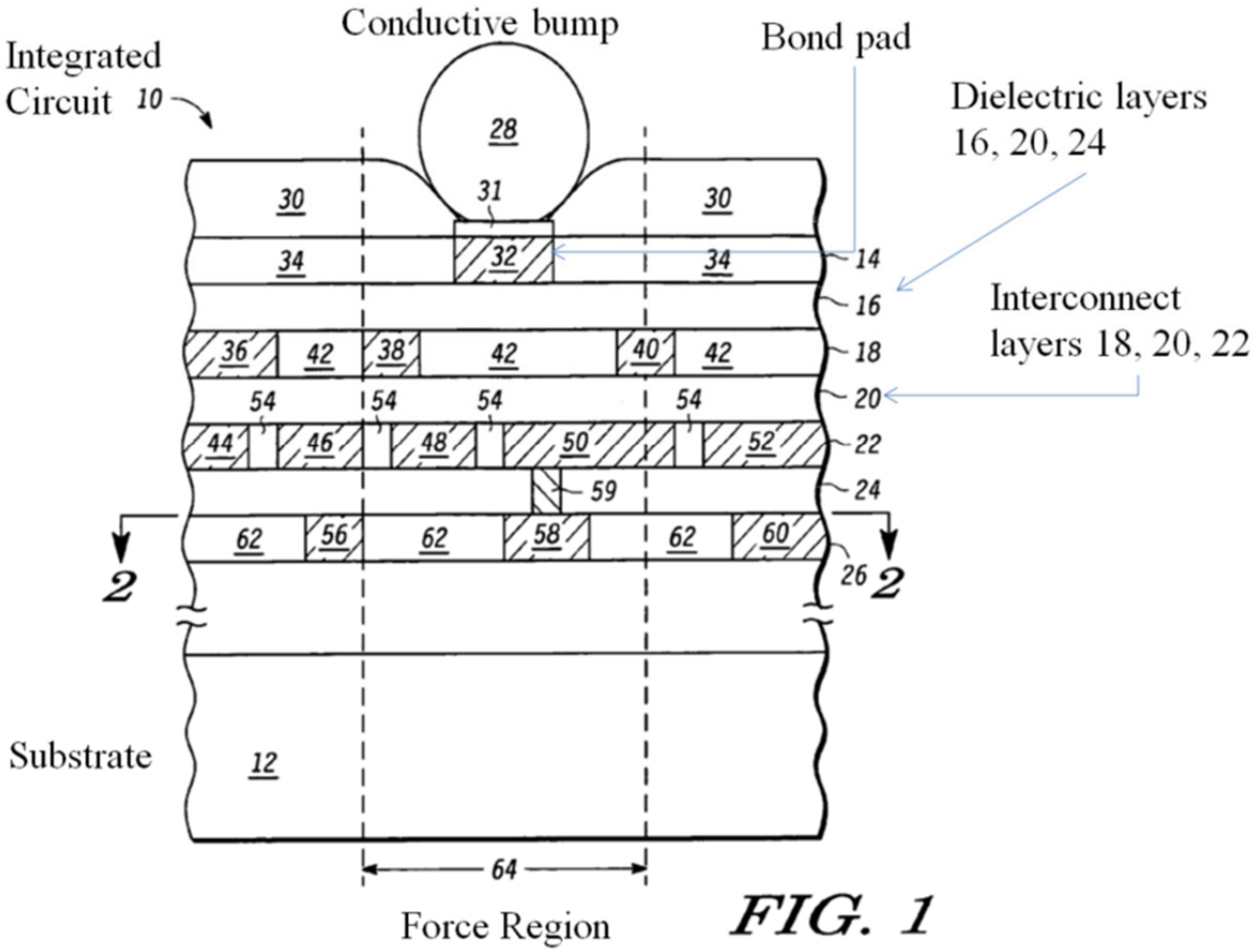

FIG. 1